[0019] Fig. 3G is a circuit diagram of the array of Fig. 3A.

[0020] Figs. 4-7, 8A, 8B, 9-12, 13A, 13B, 14A, 14B, 15A show vertical cross sections of memory structures in the process of fabrication according to one embodiment of the present invention.

[0021] Fig. 15B is a top view of a memory structure in the process of fabrication according to one embodiment of the present invention.

[0022] Figs. 15C, 16A, 16B, 16C show vertical cross sections of memory structures in the process of fabrication according to one embodiment of the present invention.

[0023] Fig. 17A is a top view of a memory structure in the process of fabrication according to one embodiment of the present invention.

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[0024] Figs. 17B, 17C, 18A, 18B, 18C, 19, 20A, 20B, 21, 22A, 22B, 22C, 23A, 23B, 23C, 24A, 24B, 24C, 25A, 25B, 26A, 26B, 27A, 27B, 28A, 28B, 29, 30, 31 show vertical cross sections of memory structures in the process of fabrication according to one embodiment of the present invention.

DESCRIPTION OF SOME EMBODIMENTS

[0025] The embodiments described in this section illustrate but do not limit the invention. The invention is not limited to particular materials, process steps, or dimensions. The invention is defined by the appended claims.

[0026] Figs. 3A-3F are different views of a nonvolatile memory array according to one embodiment of the present invention. Fig. 3A is a perspective view. Fig. 3F is a top view. Figs. 3B, 3C, 3D, 3E show vertical cross sections marked in Fig. 3F as X-B, Y-C, Y-D, and X-E respectively. The cross section X-B runs in the X direction (row direction) through floating gates 120 and the active areas between field dielectric regions 130. The cross section Y-C runs in the Y (column) direction through select gates 144S. The cross section Y-D runs in the Y direction through floating gates 120. The cross section X-E runs in the X direction through oxide regions 130 between select gates 144S. Fig. 3G is a circuit diagram of the array.

[0027] The circuit diagram of Fig. 3G is similar to that of Fig. 2 but each control gate line 134 provides the control gates to one column of the memory cells, and the adjacent